TEXAS INSTRUMENTS

DAC7571, DAC6571, DAC5571, DAC7574, DAC6574, DAC5574, and DAC8571 Evaluation Module

User's Guide

February 2004

Data Acquisition

SLAU117A

Preface

Read This First

About This Manual

This user's guide describes the DAC7574, DAC6574, DAC5574, DAC7571, DAC6571, DAC5571, and DAC8571 evaluation module. It covers the operating procedures and characteristics of the EVM board along with the devices that it supports.

How to Use This Manual

This document contains the following chapters:

Chapter 1 – EVM Overview

Chapter 2 – PCB Design and Performance

Chapter 3 – EVM Operation

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Data Sheets:	**Literature Number:**
DAC7574	SLAS375
DAC6574	SLAS408
DAC5574	SLAS407
DAC7571	SLAS374
DAC6571	SLAS406
DAC5571	SLAS405
DAC8571	SLAS373A
REF02	SBVS-003A
OPA627	PDS-998H

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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
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		Telephony	www.ti.com/telephony
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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V - V_{DD} +0.3 V and the output voltage range of ±10 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Chapter 1

EVM Overview

This chapter provides an overview of the DAC7574, DAC6574, DAC5574, DAC7571, DAC6571, DAC5571, and DAC8571 evaluation module (EVM), and instructions on setting up and using this module.

Topic **Page**

1.1 Features

This EVM features the DAC7574, DAC6574, DAC5574, DAC7571, DAC6571, DAC5571, and DAC8571 digital-to-analog converter (DAC). It provides a quick and easy way to evaluate the functionality and performance of the high-resolution as well as the low-resolution I^2C-input DACs. Although the EVM supports seven DAC types, only the selected DAC and its associated components are installed to simplify configuration. The table below shows the seven DAC types this EVM supports. The EVM also provides an I^2C serial interface to communicate with any host microprocessor or TI DSP base system.

Table 1-1. Featured DAC Selections

EVM Version	Installed Device (DUT)	DAC Channels	Resolution
DAC5571 EVM	DAC5571IDBVT	1	8-Bit
DAC5574 EVM	DAC5574IDGS	4	8-Bit
DAC6571 EVM	DAC6571IDBVT	1	10-Bit
DAC6574 EVM	DAC6574IDGS	4	10-Bit
DAC7571 EVM	DAC7571IDBVT	1	12-Bit
DAC7574 EVM	DAC7574IDGS	4	12-Bit
DAC8571 EVM	DAC8571IDGK	1	16-Bit

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The dc power supply for the digital section (V_{DD}) of this EVM is selected between 3.3 V and 5 V via the 3-position jumper W14. The digital power connects to the J5-1, J6-9, or J6-10 terminal (when plugged in with another EVM board or interface card) and is referenced to ground through the J5-2 and J6-5 terminals. The 5 V V_{DD} can also come directly from J5-1, bypassing W14. Therefore, if V_{DD} must be powered by 3.3 V via J6-9, any source connected through J5-1 must be disconnected to prevent damage to the EVM or other equipment.

Caution

To avoid potential damage to the EVM board or equipments, make sure that any cable connected to J5-1 is disconnected prior to supplying 3.3 V V_{DD} via J6-9 terminal.

The dc power supply requirements for the analog section of this EVM are as follows; the V_{CC} and V_{SS} supplies, typically ±15 V, can range from ±4.5 V to ±18 V. V_{CC} and V_{SS} connect through J1-3 and J1-1 respectively, or through J6-1 and J6-2 terminals. 5 VA connects through J5-3 or J6-3 and 3.3 VA connects through J6-8. All of the analog power supplies are referenced to analog ground through J1-2 and J6-6 terminals.

The analog power supply for the device under test (U1, U4, or U8) can be provided by either 5 VA (via J5-3 or J6-3) or by U3 through a resistor potentiometer, R11, by selecting the proper position of jumper W1. Although the digital and analog supplies are separate on the EVM to allow flexibility in supply evaluation, the supplies are treated as one, and considered analog since the DUT does not have separate analog and digital supply pins.

The V_{CC} supply source provides the positive rail of the external output op-amp (U2) and the voltage reference (U3). The negative rail of U2 can be selected between V_{SS} and AGND via W5 jumper. The external op-amp is installed as an option to provide output signal conditioning, or for other output configurations.

1.2.2 Reference Voltage

The 5-V precision voltage reference is provided to supply the external voltage reference for the DAC8571 only through REF02, U3, via jumper TP9 by shorting pins 1 and 2. The reference voltage goes through an adjustable 5-kΩ potentiometer R11 in series with 0-Ω R10, to allow the user to adjust the reference voltage.

Caution

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

Header J4 pin 20 provides a connection point for an alternative external reference source if desired. In this configuration the jumper on TP9 must be removed and TP8 must be shorted. The external voltage reference must not exceed 5 V.

The REF02 circuit also provides an alternative adjustable analog supply for U1, U4, and U8 (whichever is installed on the EVM) through W1 pin 1 if desired. It also provides both reference and supply voltages for U4 by shorting TP9.

Since it is possible to install all DAC devices (U1, U4 and U8) on the EVM, the possibility of different supply requirements may arise. To isolate the supply and reference voltages of U4 from U1 and U8, remove R25 and install R38. This allows the DAC8571 (U4) to operate using the REF02 (U3) as its supply and reference sources while U1 and U8 are supplied by 5 VA.

The REF02 precision reference is powered by V_{CC} (+15V) through J1-3 or J6-1.

Caution

When applying an external voltage reference through J4-20, make sure that it does not exceed +5 V maximum. Otherwise, this can permanently damage the DAC8571, U4, device under test.

1.3 EVM Basic Functions

This EVM is a functional platform to evaluate the features and characteristics of the DAC7574, DAC6574, DAC5574, DAC7571, DAC6571, DAC5571, and DAC8571 digital-to-analog converters. The EVM can be used with a microprocessor, TI DSP, or a waveform generator.

Headers J2 and P2 connect the control signals and data interface of a host processor or waveform generator to the DAC EVM.

A specific adapter interface card is also available for most of TI's DSP Starter Kits (DSK). The card model depends on the type of TI DSP Starter Kit to be used. When ordering an adapter interface card, specify the DSP that will be used.

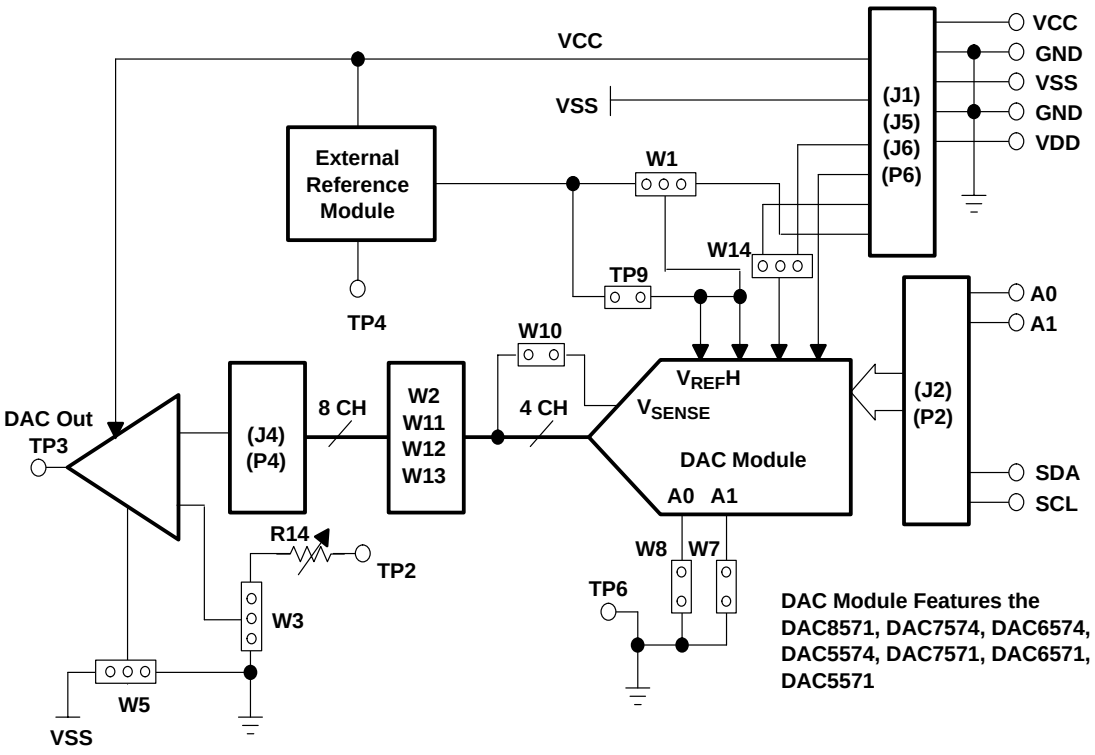
In addition, an MSP430-based platform (HPA449) that uses the MSP430F449 microprocessor can be used with this EVM. For more information regarding the adapter interface card or the HPA449 platform, please call Texas Instruments Inc. or email us at dataconvapps@list.ti.com.

The DAC outputs can be monitored through selected pins of J4. The outputs of U1 can be switched using their respective jumpers W2, W11, W12, and W13, for stacking, while U4 or U8 uses only W2. Stacking allows a total of eight DAC channels (if two DACx574 EVMs are stacked) or two DAC channels (if two DACx571 EVM are stacked) to be used provided that the I^2C address is unique for each stacked EVM board.

Any DAC output can be connected to the noninverting input of op-amp U2 by using a jumper across the appropriate pins of J4 (See EVM schematic diagram). U2 must be configured correctly for the desired waveform characteristic. (Refer to Chapter 3 of this user's guide.)

A block diagram of the EVM is shown in Figure 1-1.

Figure 1-1. EVM Block Diagram



Chapter 2

PCB Design and Performance

This chapter describes the physical and mechanical characteristics of the EVM and compares the performance of the EVM with the device data sheets. The bill of materials is also included in this chapter.

Topic **Page**

2.1 PCB Layout

The DAC EVM demonstrates the high performance of the DAC under test conditions specified in the datasheet by implementing design practices that preserve DAC performance. Careful analysis of these practices is the key to a successful design implementation. Many of the practices affect the schematic design phase, including correct component selection, adequate bypassing, separating and managing analog and digital signals, and understanding component mechanical attributes.

The circuit layout is critical in any high-performance analog circuit, and DAC circuit design is no exception. Component placement and signal routing are important considerations. Place bypass capacitors as close as possible to the pins, with analog and digital signals properly separated from each other.

The power and ground planes are very important and must be carefully designed. A solid plane is best, but when solid planes are not possible, a split plane is usually adequate. When considering a split plane design, analyze the component placement and carefully divide the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that contribute to DAC output errors. To ensure that return currents are handled properly, route the signals only in their respective sections; analog traces must only lie directly above or below the analog section and digital traces in the digital section. Minimize the length of the traces but use the widest allowable trace in the design. The EVM layout incorporates these design practices and are shown in the illustrations presented below.

This DAC EVM board is constructed on a four-layer printed circuit board using a copper-clad FR-4 laminate material. The printed circuit board dimensions are 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2500 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 2-1 through Figure 2-7 shows the artwork for the individual layers.

Figure 2-1. Top Silkscreen

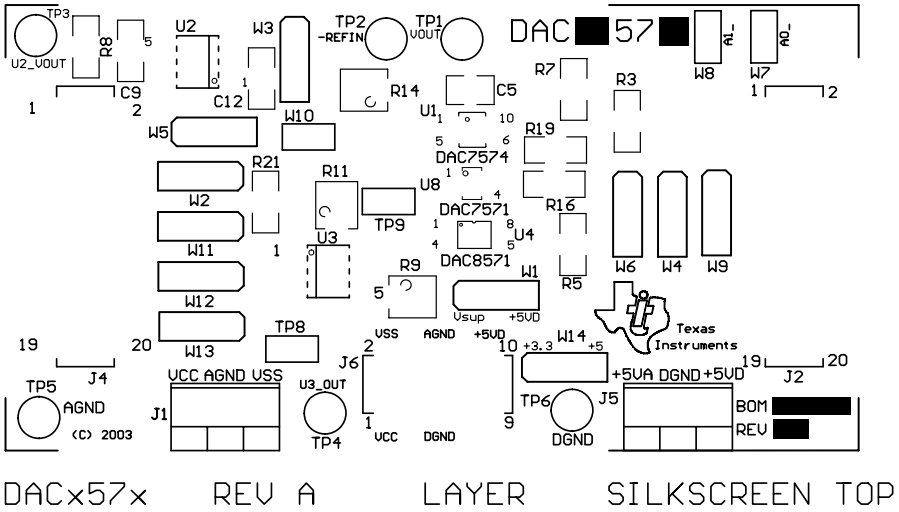


Figure 2-2. Layer 1 (Top Signal Plane)

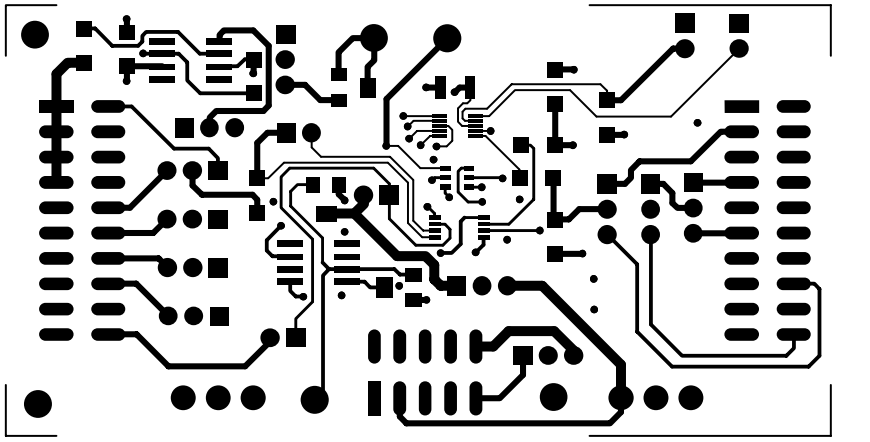


Figure 2-3. Layer 2 (Ground Plane)

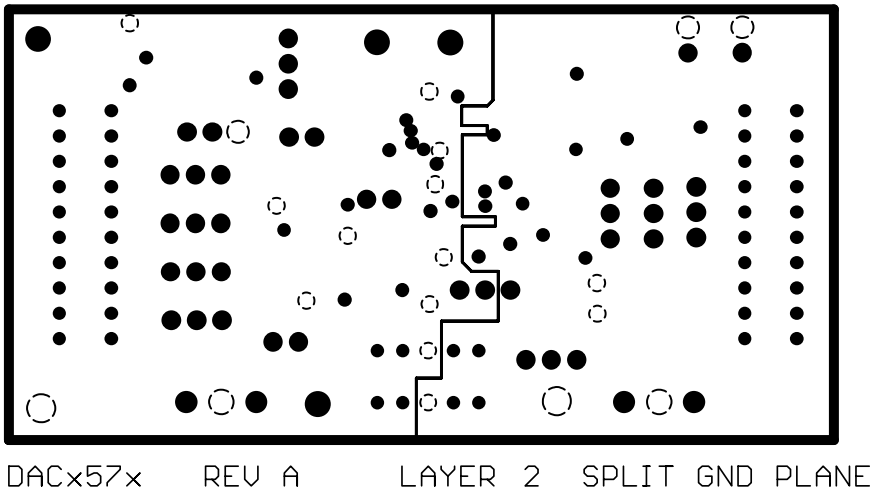


Figure 2-4. Layer 3 (Power Plane)

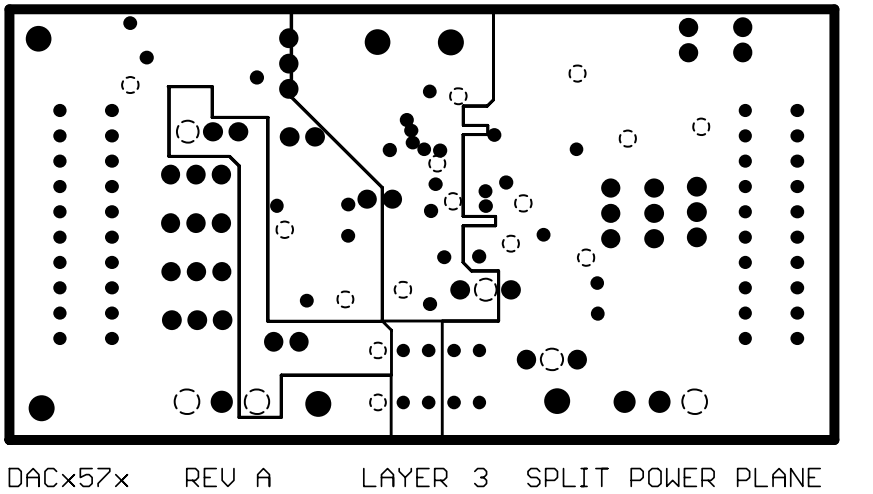


Figure 2-5. Layer 4 (Bottom Signal Plane)

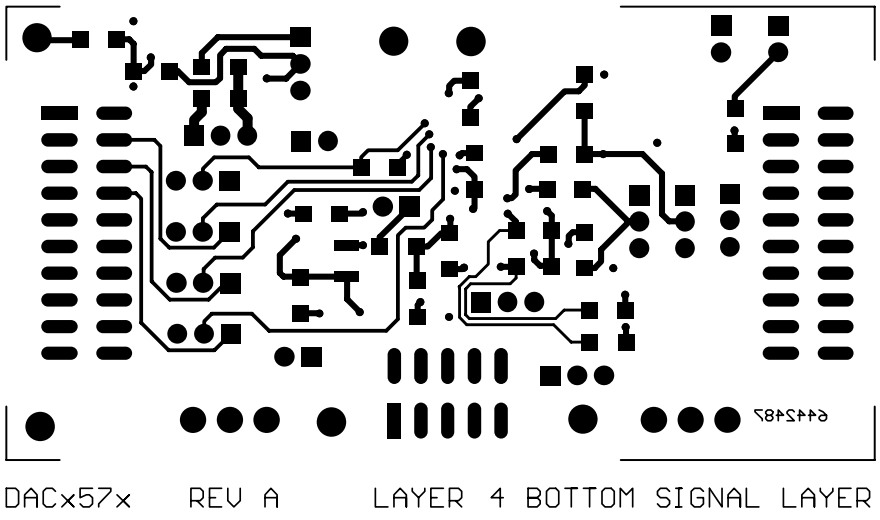


Figure 2-6. Bottom Silkscreen

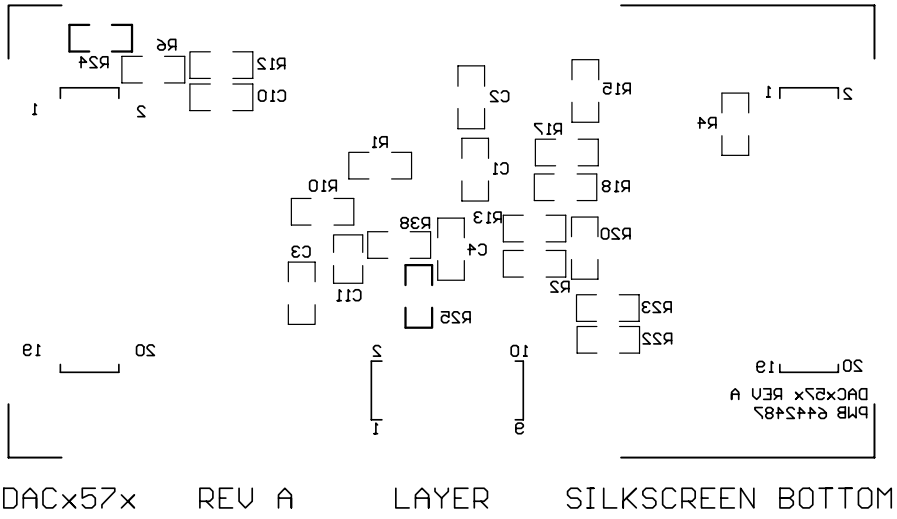
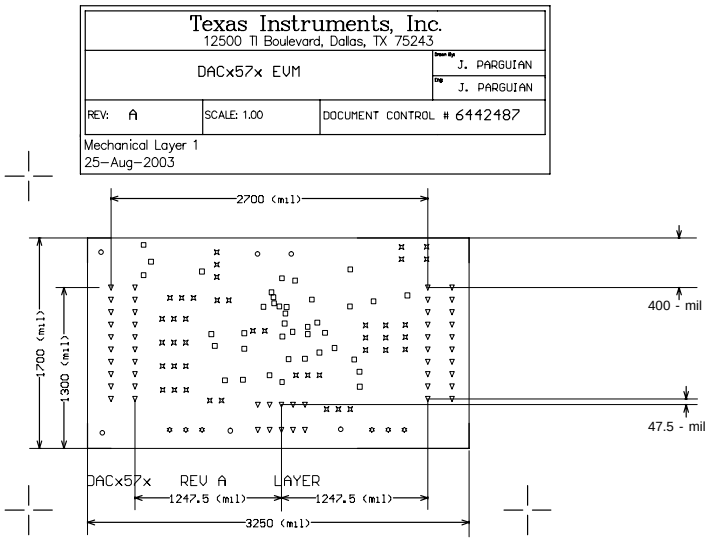


Figure 2-7. Drill Drawing



Notes:

1. PWB to be fabricated to meet or exceed PC-6012, class 3 standards and workmanship shall conform to IPC-A-600, class 3 - current revisions.
2. Board material and construction to be UL approved and marked on the finished boards.
3. Laminate Material: Copper-clad FR-4
4. Copper weight: 1oz finished
5. Finished thickness: .062 ± .010
6. Min plating thickness in through holes: .001"
7. SMOBC / HASL
8. LIP soldermask both sides using appropriate layer artwork: COLOR = GREEN
9. LIP silkscreen as required: COLOR = WHITE
10. Vender information to be incorporated on back side whenever possible
11. Minimum copper conductor widyh is: 10 MILS minimum conductor spacing is: 8 MILS
12. Number of finished layers: 4

Δ	50	13 mil	0.3302 mm	PTH
□	40	15 mil	0.381 mm	PTH
☆	45	37 mil	0.9398 mm	PTH
★	6	47.244 mil	1.2 mm	PTH
○	6	62 mil	1.5748 mm	PTH
	145	Total		

2.2 EVM Performance

EVM performance is tested using a high-density DAC bench test board, an Agilent 3458A digital multimeter, and a PC running National Instruments LABVIEW software. The EVM board is tested for all codes of the device under test (DUT) and is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

The parameters and results of the DAC EVM characterization test for the DAC7574 are shown in Figures 2-8 through 2-12. Test parameters and results for the DAC8571 are shown in Figures 2-13 and 2-14.

The characterization-test data for the DAC7571, DAC6574, DAC6571, DAC5574, and DAC5571 are not shown; it is assumed that their performance is comparable to or better than that of the DAC7574 EVM.

Figure 2-8. DAC7574EVM Test Parameters and Results

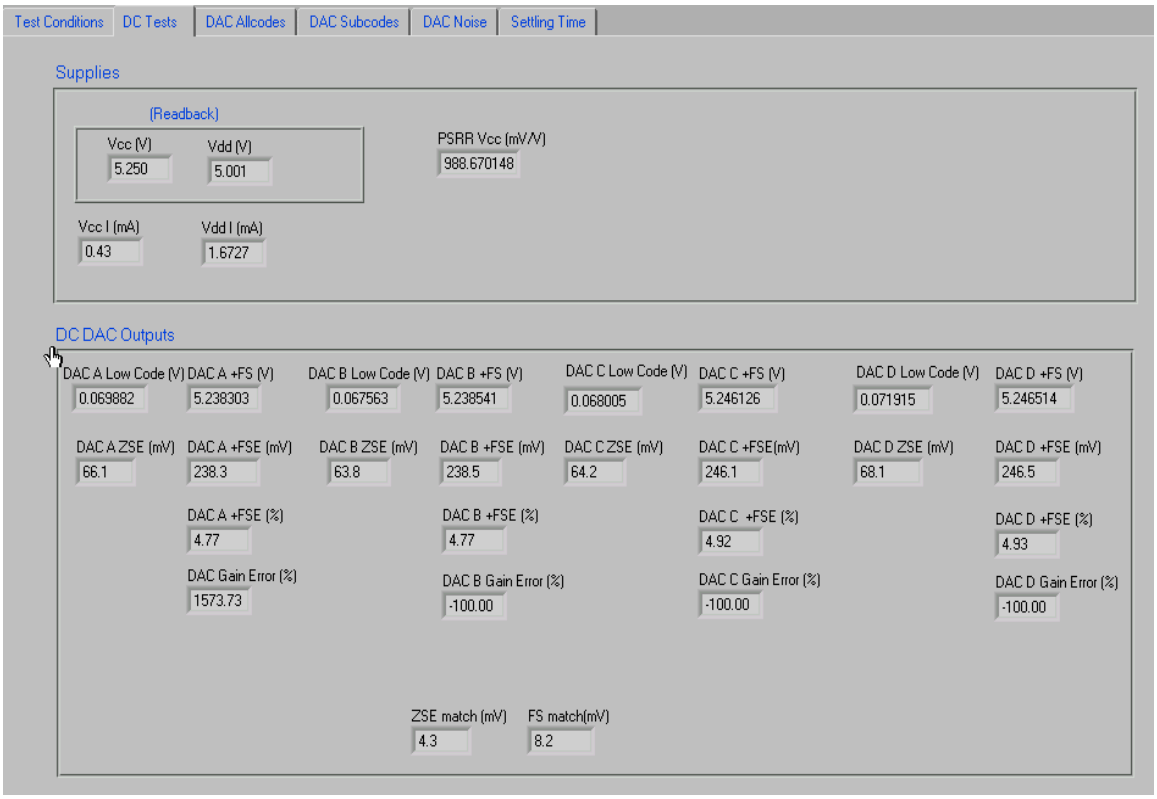


Figure 2-9. INL and DNL Characterization Graph of DAC7574 Channel A

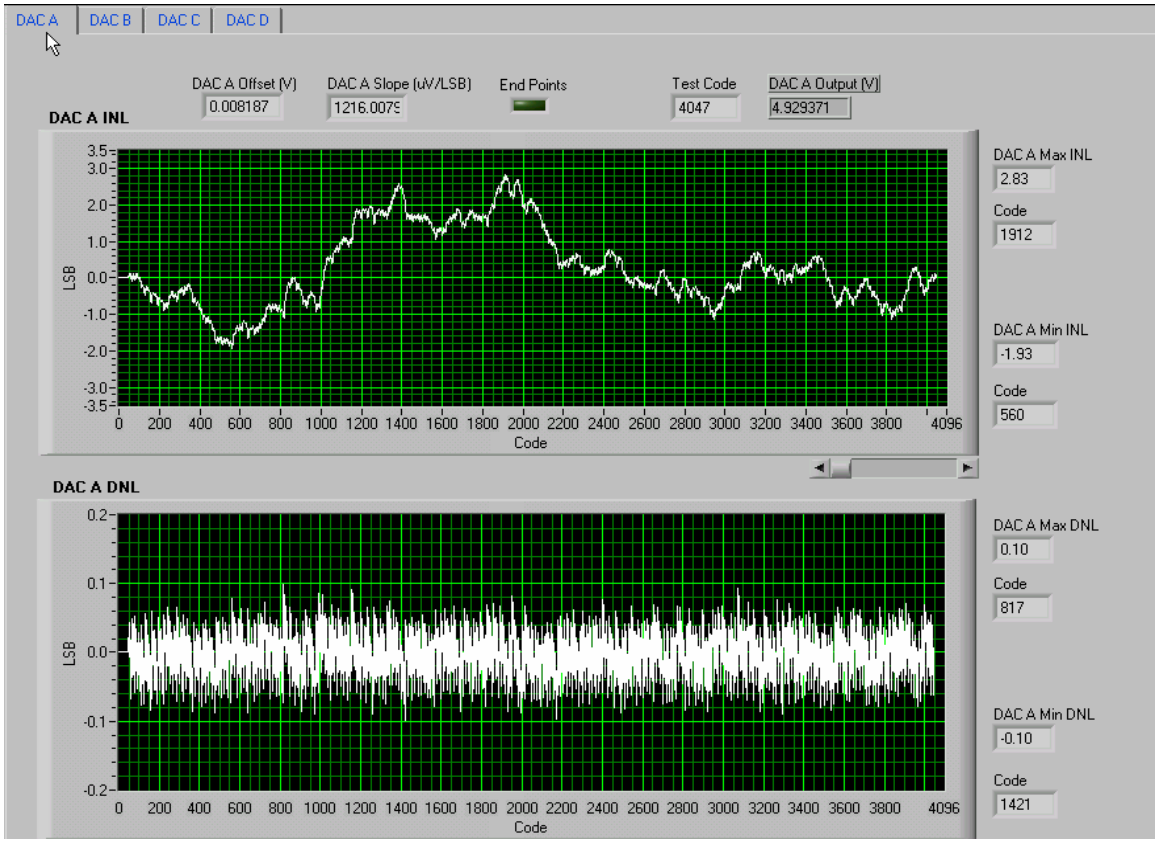


Figure 2-10. INL and DNL Characterization Graph of DAC7574 Channel B

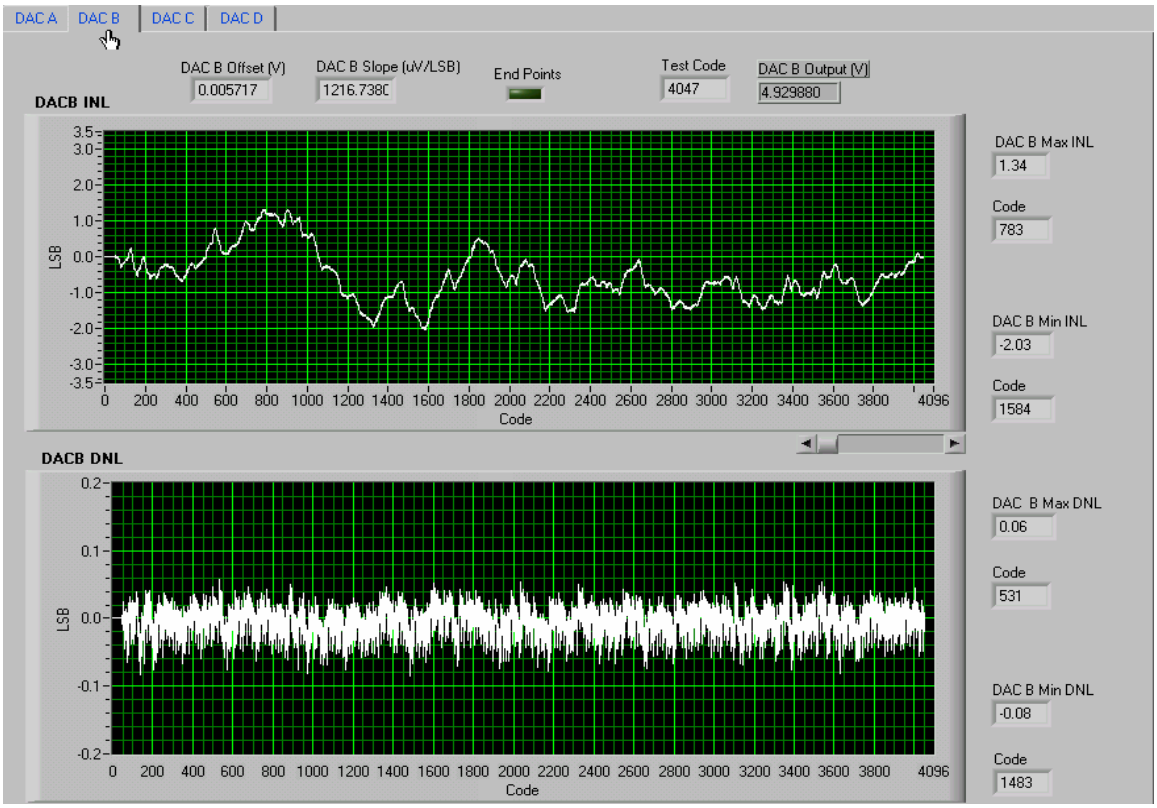


Figure 2-11. INL and DNL Characterization Graph of DAC7574 Channel C

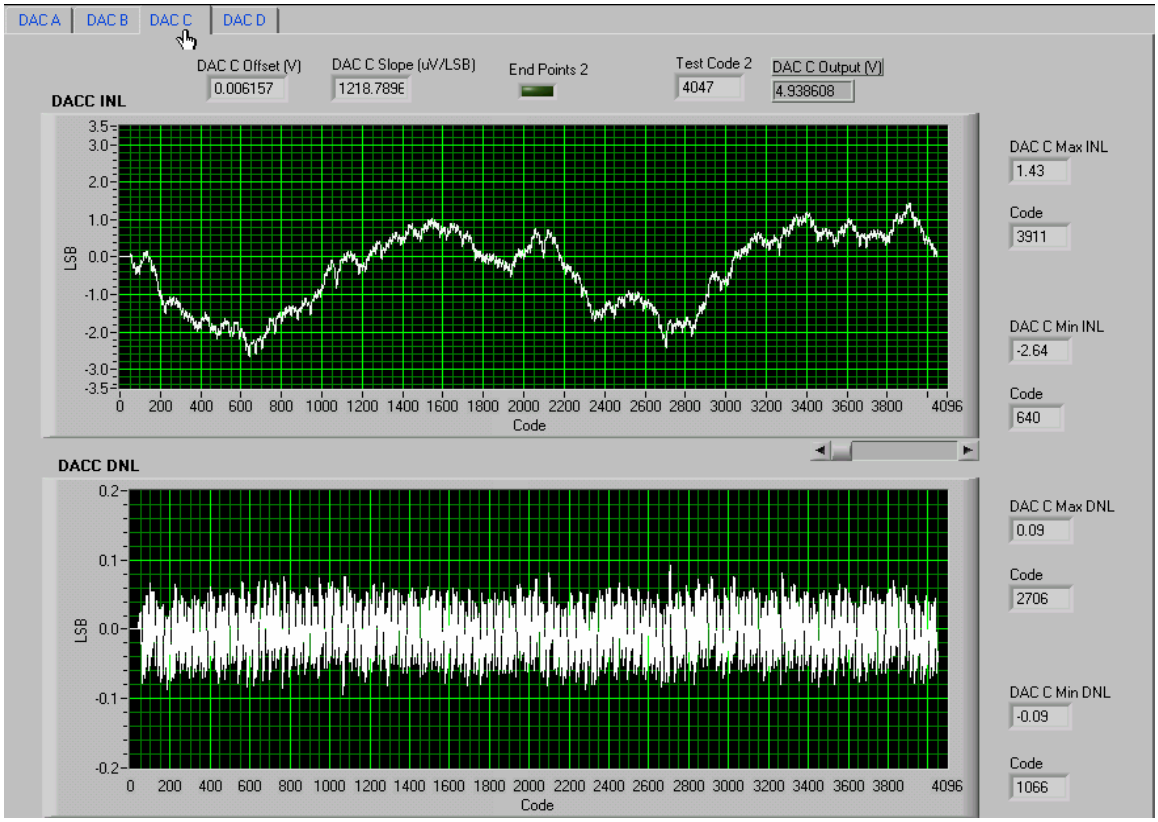


Figure 2-12. INL and DNL Characterization Graph of DAC7574 Channel D

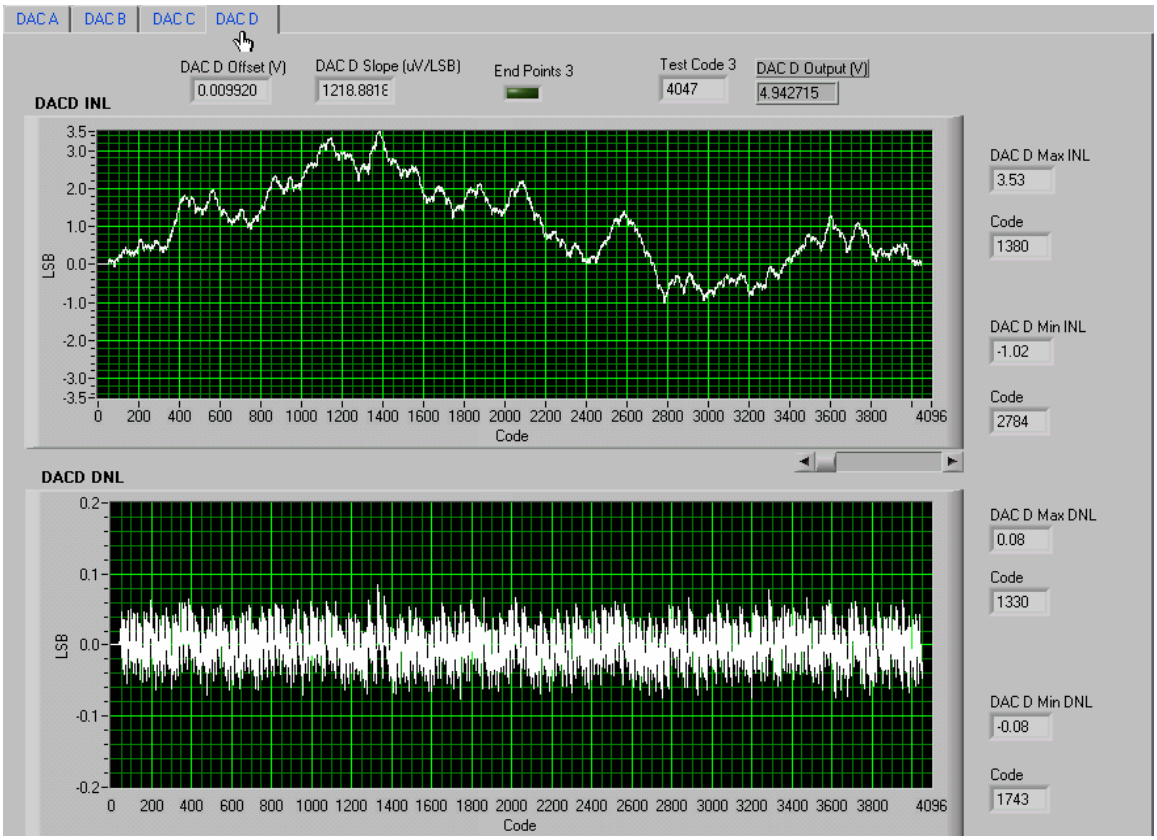


Figure 2-13. DAC8571EVM Test Parameters and Results

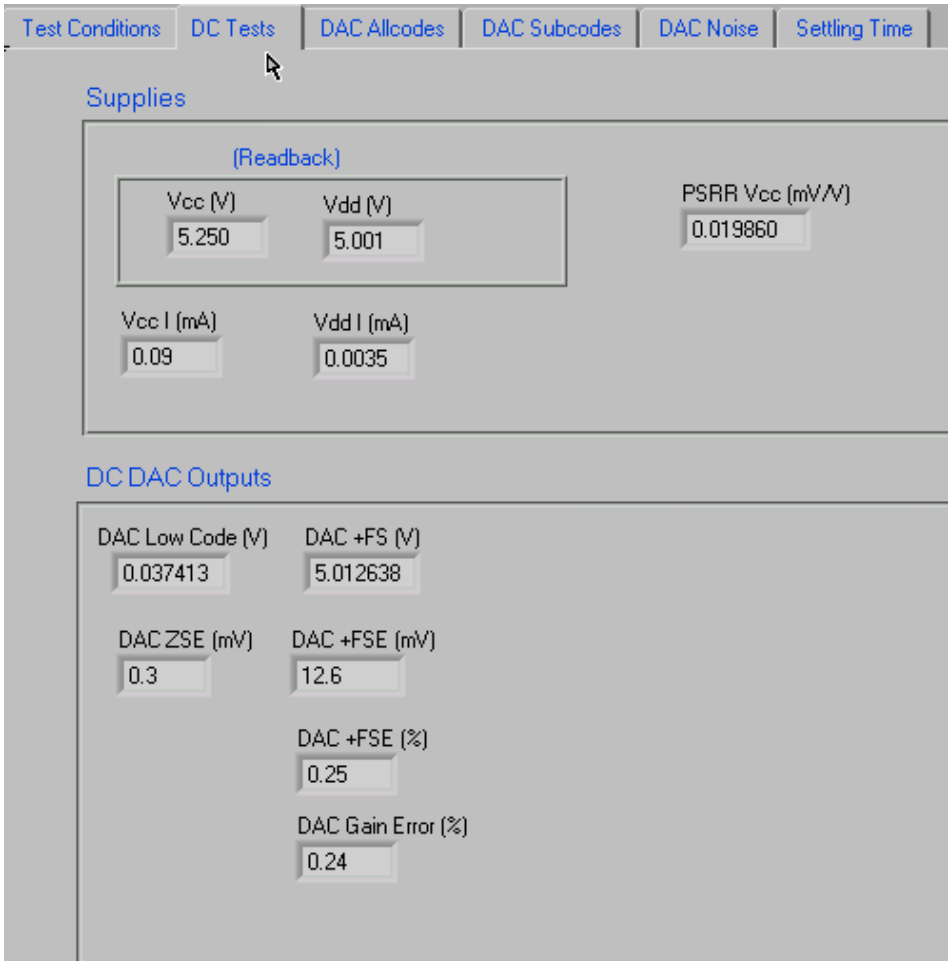
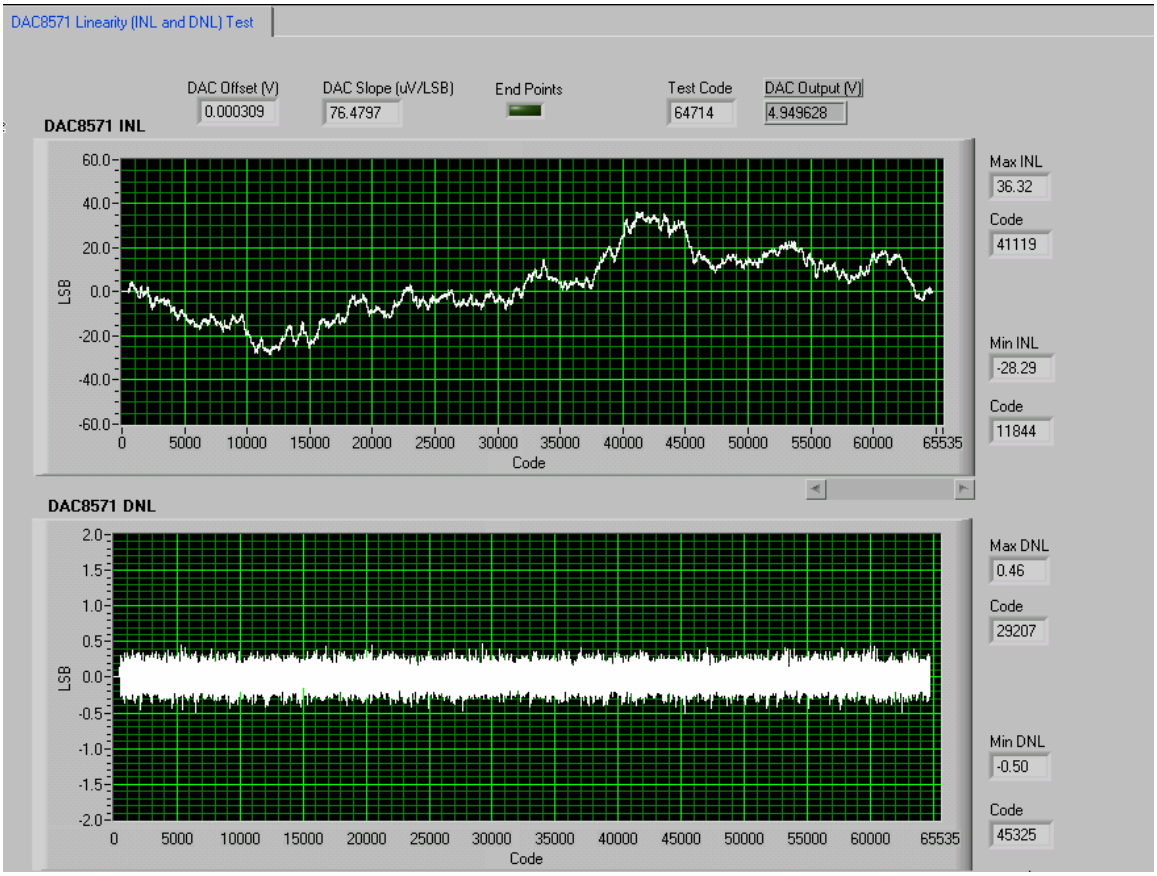


Figure 2-14. INL and DNL Characterization Graph of DAC8571



2.3 Bill of Materials

Table 2-1. Parts List

Item #	Qty	Designator	Mfr.	Part Number	Description
1	2	C9 C10	Panasonic	ECUV1H103KBM	0.01-μF, 1206 multilayer ceramic capacitor
2	4	C1 C2 C3 C4	Panasonic	ECJ3VB1C104K	0.1-μF, 1206 multilayer ceramic capacitor
3	1	C12	Panasonic	ECUV1H102JCH	1-nF, 1206 multilayer ceramic capacitor
4	2	C5 C11	Kemet	C1210C106K8PAC	10-μF, 1210 multilayer ceramic X5R capacitor
5	8	R1 R8 R10 R21 R22 R23 R25 R38	Panasonic	ERJ-8GEY0R00V	0-Ω, 1/4-W 1206 chip resistor
6	6	R15 R16 R17 R18 R19 R20	Panasonic	ERJ-8GEYJ431V	430-Ω, 1/4-W 1206 chip resistor
7	1	R24	Panasonic	ERJ-8GEYJ101V	100-Ω,1/4-W 1206 chip resistor
8	1	R10	Panasonic	ERJ-8ENF2002V	20-kΩ,1/4-W 1206 chip resistor
9	6	R2 R3 R4 R5 R7 R13	Panasonic	ERJ-8GEYJ302V	3-kΩ, 1/4-W 1206 chip resistor
10	2	R6 R12	Panasonic	ERJ-8ENF1002V	10-kΩ,, 1/4-W 1206 chip resistor
11	1	R9	Bourns	3214W-203E	20-kΩ, BOURNS_32X4W series 5T pot
12	1	R14	Bourns	3214W-103E	10-kΩ, BOURNS_32X4W series 5T pot
13	1	R11	Bourns	3214W-502E	5-kΩ,, BOURNS_32X4W series 5T pot
14	1	J6	Samtec	TSM-105-01-T-DV	5X2X0.1, 10-pin 3 A isolated power socket
15	2	J2 J4	Samtec	TSM-110-01-S-DV-M	10X2X.1, 20 Pin 0.025” sq SMT socket
16	2	J1 J5	On-Shore Technology	ED555/3DS	3-pin terminal connector
17	1	U1	Texas Instruments	DAC7574IDGS	12-bit, quad voltage output, serial input I^2C DAC, MSOP-10
				DAC6574IDGS	10-bit, quad voltage output, serial input I^2C DAC, MSOP-10
				DAC5574IDGS	8-bit, quad voltage output, serial input I^2C DAC, MSOP-10
18	1	U2	Texas Instruments	OPA627AU	8-SOP(D) precision op amp
19	1	U3	Texas Instruments	REF02AU	5-V, 8-SOP(D) precision voltage reference
20	1	U4	Texas Instruments	DAC8571IDGK	16-bit, voltage output, serial input I^2C DAC, MSOP-8
21	1	U8	Texas Instruments	DAC7571IDBVT	12-bit, voltage output, serial input I^2C DAC, SOT23-6
				DAC6571IDBVT	10-bit, voltage output, serial input I^2C DAC, SOT23-6
				DAC5571IDBVT	8-bit, voltage output, serial input I^2C DAC, SOT23-6
22	6	TP1 TP2 TP3 TP4 TP5 TP6	Mill-max	2348-2-01-00-00-07-0	Turret terminal test point
23	2	P2 P4 (see Note)	Samtec	SSW-110-22-S-D-VS-P	20-pin 0.025” square SMT terminal strips
24	1	P6 (see Note)	Samtec	SSW-105-F-D-VS-K	3-A isolated 10-pin power header
25	5	W7 W8 W10 TP8 TP9	Molex	22-03-2021	2 position jumper, 0.1” spacing
26	11	W1-W6 W9 W11-W14	Molex	22-03-2031	3 position jumper, 0.1” spacing

Note: P2, P4, and P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PC board opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2. Not all parts listed in the BOM are installed in the EVM as they are specific to the DUT installed.

Chapter 3

EVM Operation

This chapter details the operation of the EVM to guide the user in evaluating the onboard DAC and in interfacing the EVM to a host processor.

Refer to the specific DAC data sheet, as listed in the *Related Documentation from Texas Instruments* section in the *Preface* of this user's guide for more information about the DAC serial interface and other related topics.

The EVM board is factory-configured to operate in the unipolar output mode.

Topic **Page**

3.1 Factory Default Setting

The EVM board is factory-configured to operate in unipolar 5-V output mode.

Table 3-1. DAC7574/DAC6574/DAC5574 EVM Factory Default Jumper Setting

DAC7574/DAC6574/DAC5574 EVM CONFIGURATION		
Reference	**Jumper Position**	**Function**
W1	2-3	Power supply for U1 is 5 VA.
W2	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
W3	OPEN	U2 is configured as unity gain op-amp.
W4	2-3	SDA is routed to SDATA.
W5	1-2	Negative supply rail of U2 op-amp is supplied with V_{SS}.
W6	2-3	SCL is routed to SCLK.
W7	OPEN	Address line, A1, is pulled high.
W8	OPEN	Address line, A0, is pulled high.
W9	OPEN	For I^2C SDA bit-bang using the DSP
W10	OPEN	For U4 use only
W11	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
W12	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
W13	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
W14	2-3	The 5 VD is routed for digital supply.
TP8	OPEN	For U4 external V_{REF} use only
TP9	OPEN	For U4 use when tying V_{DD} and V_{REF} together

Table 3-2. DAC7571/DAC6571/DAC5571 EVM Factory Default Jumper Setting

DAC7571/DAC6571/DAC5571 EVM CONFIGURATION		
Reference	**Jumper Position**	**Function**
W1	2-3	Power supply for U8 is 5 VA.
W2	1-2	DAC output is routed to J4-2.
W3	OPEN	U2 is configured as unity gain op-amp.
W4	2-3	SDA is routed to SDATA.
W5	1-2	Negative supply rail of U2 op-amp is supplied with V_{SS}.
W6	2-3	SCL is routed to SCLK.
W7	OPEN	For U1 use only
W8	OPEN	For U1 use only
W9	OPEN	For I^2C SDA bit-bang using the DSP
W10	OPEN	For U4 use only
W11	1-2	For U1 use only
W12	1-2	For U! use only
W13	1-2	For U1 use only
W14	2-3	The 5 VD is routed for digital supply.
TP8	OPEN	For U4 external V_{REF} use only
TP9	OPEN	For U4 use when tying V_{DD} and V_{REF} together

Table 3-3. DAC8571EVM Factory Default Jumper Setting

DAC8571 EVM CONFIGURATION		
Reference	**Jumper Position**	**Function**
W1	2-3	Power supply for the DAC8571 is 5 VA.
W2	1-2	DAC output is routed to J4-2.
W3	OPEN	U2 is configured as unity gain op-amp.
W4	2-3	SDA is routed to SDATA..
W5	1-2	Negative supply rail of U2 op-amp is supplied with $V_{SS.}$
W6	2-3	SCL is routed to SCLK.
W7	OPEN	For U1 use only
W8	OPEN	For U1 use only
W9	OPEN	For I^2C SDA bit-bang using the DSP
W10	CLOSE	V_{SENSE} is tied to V_{OUT} for feedback.
W11	1-2	For U1 use only
W12	1-2	For U1 use only
W13	1-2	For U1 use only
W14	2-3	The 5 VD is routed for digital supply.
TP8	OPEN	For connecting external V_{REF} if desired
TP9	OPEN	For tying V_{DD} and V_{REF} together and isolating it from U1 and U8 (if all DUTs are installed)

3.2 Host Processor Interface

Because the host processor controls the DAC, proper operation depends on the correct interface of the host processor and the EVM board. Properly written code is also required to operate the DAC.

A host-platform-specific cable assembly connects the EVM to the host processor through J2 for the I^2C serial-control and data signals. The output is monitored through J4.

An interface-adapter card is available for specific TI DSP starter kits as well as for an MSP430 based microprocessor as mentioned in Chapter 1, section 1.3. Using the interface card alleviates the tedious task of building custom cables and allows easy configuration of a simple evaluation system.

This DAC EVM interfaces with any host processor capable of I^2C protocols or the popular TI DSP. For more information regarding the serial interface of the particular DAC installed, please refer to the specific DAC datasheet, as listed in the *Related Documentation from Texas Instruments* section in the *Preface* of this user's guide.

3.3 EVM Stacking

EVM stacking enables the designer to evaluate two DACx574s in tandem to yield an eight channel output, or two DACx571s, or two DAC8571s. Any combination of the seven may be used provided the outputs do not collide. A maximum of two DACx574 EVMs are allowed since the output terminal, J4, dictates the number of DAC channels that can be connected without colliding. For the DACx571 and DAC8571, more than two EVMs can be stacked together provided the I^2C address of each stacked EVMs are unique, as the outputs can be monitored through TP1 instead of shorting W2 jumper and routing the DAC output to J4. Table 4 shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper position of W2, W11, W12, and W13.

Table 3-4. DAC7571/DAC6571/DAC5571 Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	U8 output (V_{OUT}) is routed to J4-2.
	2-3	U8 output (V_{OUT}) is routed to J4-10.

Table 3-5. DAC8571 Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	U4 output (V_{OUT}) is routed to J4-2.
	2-3	U4 output (V_{OUT}) is routed to J4-10.

Table 3-6. DAC7574/DAC6574/DAC5574 Output Channel Mapping

Reference	Jumper Position	Function
W2	1-2	U1 output A ($V_{OUT}A$) is routed to J4-2.
	2-3	U1 output A ($V_{OUT}A$) is routed to J4-10.
W11	1-2	U1 output B ($V_{OUT}B$) is routed to J4-4.
	2-3	U1 output B ($V_{OUT}B$) is routed to J4-12.
W12	1-2	U1 output C ($V_{OUT}C$) is routed to J4-6.
	2-3	U1 output C ($V_{OUT}C$) is routed to J4-14.
W13	1-2	U1 output D ($V_{OUT}D$) is routed to J4-8.
	2-3	U1 output D ($V_{OUT}D$) is routed to J4-16.

Each DAC EVM in a stacked configuration must have a unique I^2C address. This is accomplished by configuring the address jumpers W7 and W8 (refer to the datasheet for I^2C addressing) for the DACx574 EVM. The DACx571 and DAC8571 use pullup and pulldown resistors R13, R22, R2, and R23 respectively. The table below shows the I^2C address settings of each EVM. The cells shaded in gray are factory preset and cannot be changed.

Table 3-7. DAC7574/DAC6574/DAC5574 I²C Slave Address Map

Factory Set I²C Address					W7	W8	R/$\overline{W}$	I²C Address and Function
1	0	0	1	1	Open	Open	0	0x9E (Write)
1	0	0	1	1	Open	Close	0	0x9C (Write)
1	0	0	1	1	Close	Open	0	0x9A (Write)
1	0	0	1	1	Close	Close	0	0x98 (Write)
1	0	0	1	1	Open	Open	1	0x9F (Read)
1	0	0	1	1	Open	Close	1	0x9D (Read)
1	0	0	1	1	Close	Open	1	0x9B (Read)
1	0	0	1	1	Close	Close	1	0x99 (Read)

Table 3-8. DAC7571/DAC6571/DAC5571 I²C Slave Address Map

Factory Set I²C Address						Address Resistor	R/$\overline{W}$	I²C Address and Function
1	0	0	1	1	0	R22 installed R13 installed	0	0x98 (Write)
1	0	0	1	1	0	R22 not installed R13 installed	0	0x9A (Write)
1	0	0	1	1	0	R22 installed R13 installed	1	0x99 (Read)
1	0	0	1	1	0	R22 not installed R13 installed	1	0x9B (Read)

Table 3-9. DAC8571 I²C Slave Address Map

Factory Set I²C Address					Address Resistor	See Note	R/$\overline{W}$	I²C Address and Function
1	0	0	1	1	R2 installed R23 installed	0	0	0x98 (Write)
1	0	0	1	1	R2 installed R23 not installed	0	0	0x9C (Write)
1	0	0	1	1	R2 installed R23 installed	0	1	0x99 (Read)
1	0	0	1	1	R2 installed R23 not installed	0	1	0x9D (Read)

Note: Shaded columns represent factory-set I²C address bits.

3.4 The Output Op Amp

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. Only one DAC output channel can be monitored at any given time for evaluation since the odd numbered pins (J4-1 to J4-7) are tied together. The output op-amp is configured to unity gain by default. Nevertheless, the raw outputs of the DAC can be probed through the even pins of J4, the output terminal, which also provides mechanical stability when stacking or plugging into any interface card. J4 also provides

easy access for monitoring up to eight DAC channels when stacking two DACx574 EVMs together, as described in section 3.3.

The inverting input of U2 can be tied to AGND or to any voltage source through TP2, which is selectable by the jumper configuration of W3. The voltage source connected to TP2 is adjustable via potentiometer R14.

The following sections describe various configurations of the output amplifier, U2.

3.4.1 Unity Gain Output (Default Configuration)

The buffered output configuration can be used to prevent loading the DAC. However, it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match their desired wave shape by simply removing R7 and C11 and replacing them with the desired values. R7 can be replaced with a zero-ohm resistor and C11 can be left open if desired.

Table 3-10 shows the jumper settings for the unity gain configuration of the output buffer in unipolar or bipolar supply mode.

Table 3-10. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	Open	Open	Disconnects TP2 input or AGND from the inverting input of the op-amp
W5	2-3	1-2	Supplies V_{SS} to the negative rail of op-amp or ties it to AGND

3.4.2 Output Gain of Two

Table 3-11 shows the proper jumper settings of the EVM for the 2× gain output of the DAC.

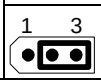
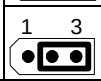
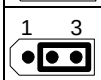
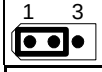
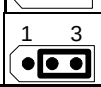
Table 3-11. Gain of Two Output Jumper Settings

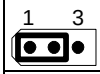
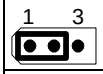
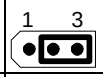
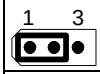
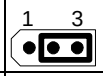
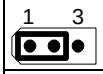
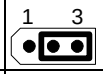
Reference	Jumper Setting		Function
	Unipolar	Bipolar	
W3	1-2	1-2	Inverting input of the output op-amp, U2, is connected to AGND to set for a gain of 2.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of op-amp, U2, for bipolar supply mode, or ties it to AGND for unipolar supply mode

3.5 Jumper Setting

Table 3-12 shows the function of each specific jumper setting of the EVM.

Table 3-12. Jumper Setting Function

Reference	Jumper Setting	Function
W1		5-V analog supply is selected for AV_{DD}.
		+3.3-V analog supply is selected for AV_{DD}.
W2		Routes $V_{OUT}A$ to J4-2
		Routes $V_{OUT}A$ to J4-10
W3		Connects AGND to the inverting input of the output op amp, U2
		Configures output op amp, U2, to unity gain
		Connects TP2 input to the inverting input of the output op amp, U2
W4		Routes the selected position of W9 jumper to SDATA input
		Routes SDA input to SDATA input
W5		Negative supply rail of the output op amp, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output op amp, U2, is tied to AGND for unipolar operation.
W6		Routes CLKX to SCLK input
		Routes SCL to SCLK input
W7		A1 pin is set high through pull-up resistor, R4. Used for U1 only.
		A1 pin is set low. Used for U1 only.
W8		A0 pin is set high through pull-up resistor, R3. Used for U1 only.
		A0 pin is set low. Used for U1 only.
W9		FSX is selected to connect to W4 for SDATA input.
		None selected
		DX is selected to connect to W4 for SDATA input.

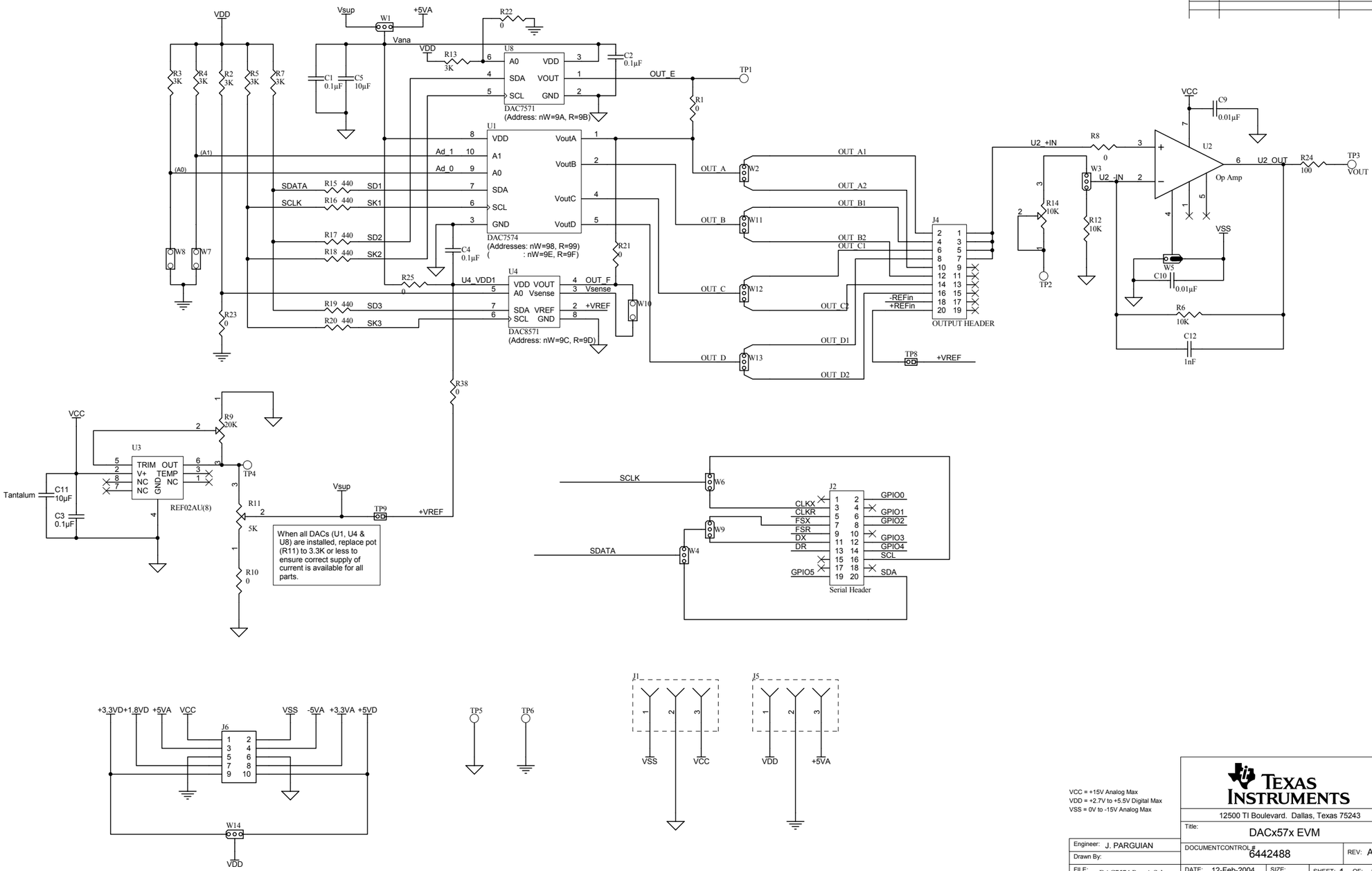
Reference	Jumper Setting	Function
W10		U4 V_{SENSE} pin is disconnected to its V_{OUT} pin.
		U4 V_{SENSE} pin is connected to its V_{OUT} pin.
W11		Routes V_{OUT}B to J4-4
		Routes V_{OUT}B to J4-12
W12		Routes V_{OUT}C to J4-6
		Routes V_{OUT}C to J4-14
W13		Routes V_{OUT}D to J4-8
		Routes V_{OUT}D to J4-16
W14		Connects 3.3 VD to VDD for digital supply
		Connects 5 VD to VDD for digital supply
TP8		Disconnects external V_{REF} to U4, reference input
		Connects external V_{REF} to U4, reference input
TP9		Disables sharing of supply and reference of U4
		Enables sharing of supply and reference of U4

Legend:  Indicates the corresponding pins that are shorted or closed.

3.6 Schematic

The schematic diagram follows this page.

Revision History		
REV	ECN Number	Approved



VCC = +15V Analog Max
VDD = +2.7V to +5.5V Digital Max
VSS = 0V to -15V Analog Max

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Engineer: J. PARGUIAN	Title: DACx57x EVM		
Drawn By:	DOCUMENTCONTROL #: 6442488		REV: A
FILE: DAC7574 Rev A.Sch	DATE: 12-Feb-2004	SIZE:	SHEET: 1 OF: 1

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